

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE APPLICATION OF:

WILLIAM J. BORLAND ET AL.

CASE NO.: **EL0496 US NA**

APPLICATION NO.: **10/663,551**

CONFIRMATION NO.: **2580**

GROUP ART UNIT: **2831**

EXAMINER:

FILED: **SEPTEMBER 16, 2003**

FOR: **PRINTED WIRING BOARDS HAVING LOW INDUCTANCE EMBEDDED
CAPACITORS AND METHODS OF MAKING SAME**

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with 37 CFR 1.97 and 1.98, Applicant would like to bring to the attention of the U.S. Patent and Trademark Office information that may be helpful in the examination of the above-identified patent application. All of the information is listed on an attached Form PTO/SB/08.

Should any fee be required in connection with the filing of this Information Disclosure Statement, please charge such fee to Deposit Account No. 04-1928 (E. I. du Pont de Nemours and Company).

Respectfully submitted,

REBECCA W. TULLOCH
ATTORNEY FOR APPLICANTS
Registration No.: 36,297
Telephone: (302) 892-7911
Facsimile: (302) 992-7343

Dated: 1/12/04

Enclosures

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	3
-------	---	----	---

Complete if Known

Application Number	10/663,551
Filing Date	September 16, 2003
First Named Inventor	William J. Borland
Art Unit	2831
Examiner Name	
Attorney Docket Number	EL0496 US NA



Substitute for form 1449B/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet

2

of

3

Complete if Known

Application Number	10/663,551
Filing Date	September 16, 2003
First Named Inventor	William J. Borland
Art Unit	2831
Examiner Name	
Attorney Docket Number	EL0496 US NA

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		JOHN FELTEN AND SAUL FERGUSON, Embedded Ceramic Resistors and Capacitors for PWB, IP Printed Circuit Expo, San Diego, CA, April 2000.	<input type="checkbox"/>
		JOHN J. FELTEN AND SAUL FERGUSON, Ceramic Resistors and Capacitors Embedded in PWB, IPC, San Diego, April 5, 2000.	<input type="checkbox"/>
		JOHN J. FELTEN AND SAUL FERGUSON, Ceramic Resistors and Capacitors Embedded in PWB, IMAPS, Denver, April 29, 2000.	<input type="checkbox"/>
		JOHN J. FELTEN AND WILLIAM J. BORLAND, Embedded Ceramic Passives in PWB: Process Development, IPC Printed Circuit Expo, Anaheim, CA, April 2001.	<input type="checkbox"/>
		JOHN J. FELTEN AND WILLIAM J. BORLAND, Ceramic Resistors and Capacitors Embedded in PWB's, IPC Expo, April 3, 2001.	<input type="checkbox"/>
		WILLIAM BORLAND, Designing for Embedded Passives, Printed Circuit Design, August 2001.	<input type="checkbox"/>

Examiner
SignatureDate
Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



PTO/SB/08b (08-03)

Approved for use through 06/30/2006. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet

3

of

3

Complete If Known

Application Number

10/663,551

Filing Date

September 16, 2003

First Named Inventor

William J. Borland

Art Unit

2831

Examiner Name

Attorney Docket Number

EL0496 US NA

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		WILLIAM BORLAND, JOHN J. FELTEN, Thick Film Ceramic Capacitors and Resistors inside Printed Circuit Boards, 34th International Symposium on Microelectronics (IMAPS), Oct. 9-11th, 2001, Baltimore, MD.	<input type="checkbox"/>
		JOHN FELTEN, RICHARD SNOGREN, JIMING ZHOU, Embedded Ceramic Resistors and Capacitors in PWB: Process and Performance, Fall IPC Meeting, October 11, 2001, Orlando, FL.	<input type="checkbox"/>
		WILLIAM J. BORLAND AND SAUL FERGUSON, Embedded Passive Components in Printed Wiring Boards, a Technology Review, To be published in CircuiTree Magazine, 2001.	<input type="checkbox"/>
		JIMING ZHOU, JOHN D. MYERS AND JOHN J. FELTEN, Embedded Passives Technology for PCBs: Materials, Design, and Process, IMAPS 2002 Conference, Denver, CO, Sept. 4-6, 2002.	<input type="checkbox"/>
		JOHN J. FELTEN, Electronic Circuits World Convention, Paper number IPC31, Advanced Embedded Passives Technologies - Putting Ceramic Components into Organic PWBs.	<input type="checkbox"/>
		WILLIAM BORLAND, JOHN J. FELTEN, SAUL FERGUSON, ALTON B. JONES AND ANGELA A. LAWRENCE, Embedded Singulated Ceramic Passives in Printed Wiring Boards, IMAPS Advanced Technology Workshop on Passive Integration, Ogunquit, ME, June 19-21, 2002.	<input type="checkbox"/>

Examiner
SignatureDate
Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



Certificate of Mailing under 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on January 12, 2004
Date

M. Kay Lilly
Signature

M. Kay Lilly

Typed or printed name of person signing Certificate

Note: Each paper must have its own certificate of mailing, or this certificate must identify each submitted paper.

10/663,551
EL0496 US NA
INFORMATION DISCLOSURE STATEMENT
FORMS PTO SB08 a, and PTO SBO8 b (2)
COPIES OF CITED REFERENCES (22)
RETURN POSTAL RECEIPT CARD
CERTIFICATE OF MAILING

This collection of information is required by 37 CFR 1.8. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.8 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.